Agilent W2630-Series

DDR2 DRAM BGA Probes

Installation Guide

Agilent Technologies

Notices

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Article I. Contents

1 Introduction

This document provides installation information for the following Agilent products:

- W2631A DDR2 x16 command and data probe
- W2632A DDR2 x16 BGA data probe
- W2633A DDR2 x8 BGA command and data probe
- W2634A DDR2 x8 BGA data probe
- E5384A adapter cable adapter for 8x16 DRAM BGA
- E5826A adapter cable for 2x16 DRAM BGA
- E5827A adapter cable for 2x8 DRAM BGA

The figures below show the overall features and connection points for the probe:

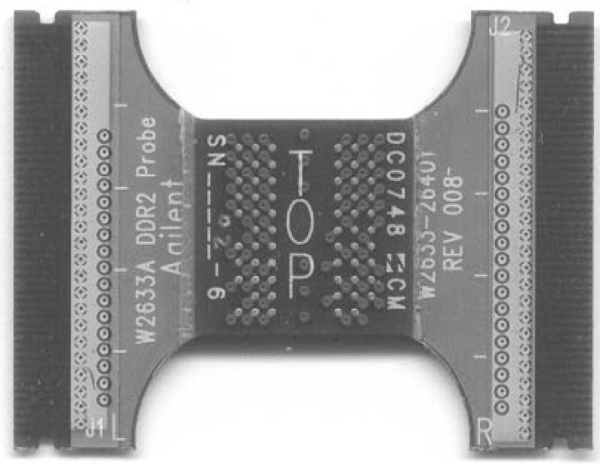

Figure 1 W2633A DDR2 x8 BGA command and data probe for logic analyzer and oscilloscope

Figure 2 E5384A 46-channel single-ended ZIF probe for x8/x16 DRAM BGA probe connects to a 90-pin logic analyzer cable

DDR2 DRAM BGA Probe Description

The DDR2 DRAM BGA probe enables logic analyzer state and timing measurements of all the DRAM buses, including the DQ, DQS, and clock signals of x8 and x16 DRAMs using the JEDEC standard common DDR2 DRAM footprint.

The probe interposes between the DRAM being probed and the PC board where the DRAM would normally be soldered. The probe is designed to be soldered to the PCB footprint for the DRAM The DRAM being probed is then soldered to the top side of the probe.

Each DRAM signal in the common footprint (including those defined for x8 and x16 DRAMs) passes directly from the bottom side of the probe to the top side of the probe. Buried probe resistors placed at the DRAM balls connect the probed signals to the rigid flex to mate with an Agilent cable adapter (ZIF probe). The W2630-series probes are also compatible with the Agilent InfiniiMax oscilloscope probes. This allows scope probing of the DRAM signals with an Infiniium 54840- or 80000-series oscilloscope, giving you a DDR2 testing solution covering the clock characterization, electrical and timing parameters of the JEDEC specification.

Fixture Technical Feature Summary

- Probing of DDR2 x8 and x16 DRAMs in BGA package using JEDEC standard common BGA footprint.
- Logic analyzer (using E5384A/E5836/7A single ended ZIF probe) and oscilloscope (using InfiniMax solder in probe head) connection to RAS, CAS, WE, DQ, DQS, DQS#, and CK/CK# signals.
- Differential or single ended probing of DQS and CLK signals.
- Interposer design probes signals between DRAM BGA balls and DIMM.
- Use of separate E5384A, E5826A or E5827A single ended probes for connection to the logic analyzer optimizes use of analyzer channels by allowing assignment of analyzer channels to 8 or 16 bits on each DRAM.
- Tin plating of the DRAM footprint on the top side of the probe is compatible with leaded and no-lead DRAM balls.

Equipment Required

This section provides the configuration guide for probing x8 and x16 DRAM type with various data width. You will need:

- Agilent 16900-series logic analysis system
- An appropriate number of Agilent logic analyzer cards connected together as a module

The following table shows how many DRAM BGA probes and cable adapters are required to provide connections to all channels of your logic analyzer module.

Table 1 Number of DRAM BGA probes and cable adapters required

DRAM	Data Width	Probes	Cables	Number of LA modules
x8	x16	W2633A	E5384A	16950B
				16950B
x8	x32	W2633A	E5384A	16950B
				16950B
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	

Table 1 Number of DRAM BGA probes and cable adapters required

DRAM	Data Width	Probes	Cables	Number of LA modules
x8	x64	W2633A	E5384A	16950B
				16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A	E5827A	16950B
x8	x72	W2633A	E5384A	16950B
				16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
x8	144	W2633A	E5384A	16950B
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A		
		W2634A	E5827A	16950B
		W2634A		
		W2634A	E5827A	
		W2634A	E5827A	16950B

Table 1 Number of DRAM BGA probes and cable adapters required

<table>
<tr><th>DRAM</th><th>Data Width</th><th>Probes</th><th>Cables</th><th>Number of LA modules</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="2">x16</td><td rowspan="2">x32</td><td>W2631A</td><td>E5384A</td><td>16950B</td></tr>
<tr><td>W2632A</td><td>E5826A</td><td>16950B</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="4">x16</td><td rowspan="4">x64</td><td>W2631A</td><td>E5384A</td><td>16950B</td></tr>
<tr><td>W2632A</td><td>E5826A</td><td rowspan="2">16950B</td></tr>
<tr><td>W2632A</td><td>E5826A</td></tr>
<tr><td>W2632A</td><td>E5826A</td><td>16950B</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="8">x16</td><td rowspan="8">x128</td><td>W2631A</td><td>E5384A</td><td>16950B</td></tr>
<tr><td>W2632A</td><td>E5826A</td><td>16950B</td></tr>
<tr><td>W2632A</td><td>E5826A</td><td rowspan="2">16950B</td></tr>
<tr><td>W2632A</td><td>E5826A</td></tr>
<tr><td>W2632A</td><td>E5826A</td><td rowspan="2">16950B</td></tr>
<tr><td>W2632A</td><td>E5826A</td></tr>
<tr><td>W2632A</td><td>E5826A</td><td rowspan="2">16950B</td></tr>
<tr><td>W2632A</td><td>E5826A</td></tr>
</table>

Mechanical Considerations

Probe Dimensions and Keep Out Volume

The following figures show the KOV of the Agilent E5384A, E5826, E5827A logic analyzer cable adapters when connected to the W2630-series DDR2 DRAM BGA probe.

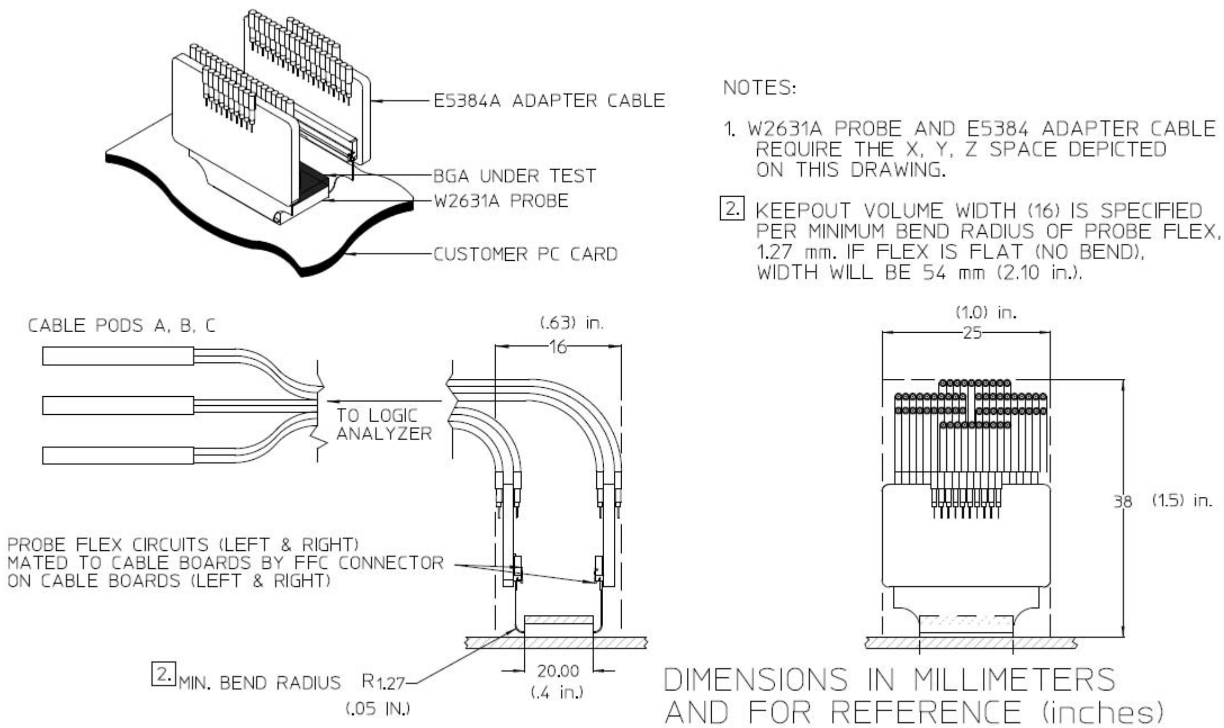

Figure 3 KOV of W2631A with E5384A

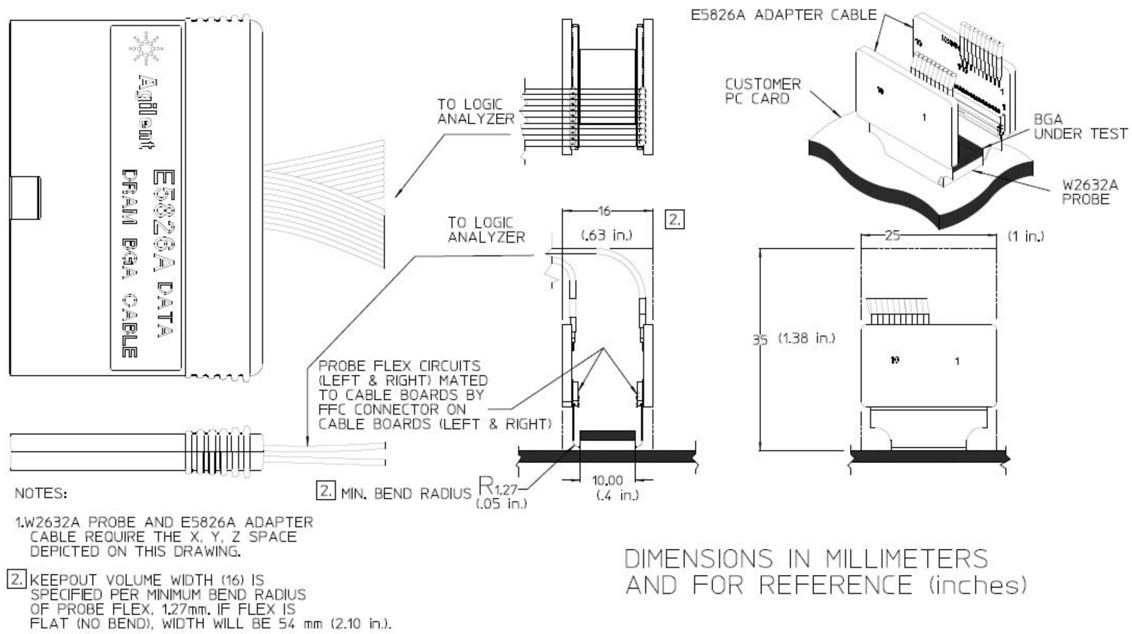

Figure 4 KOV of W2632A with E5826A

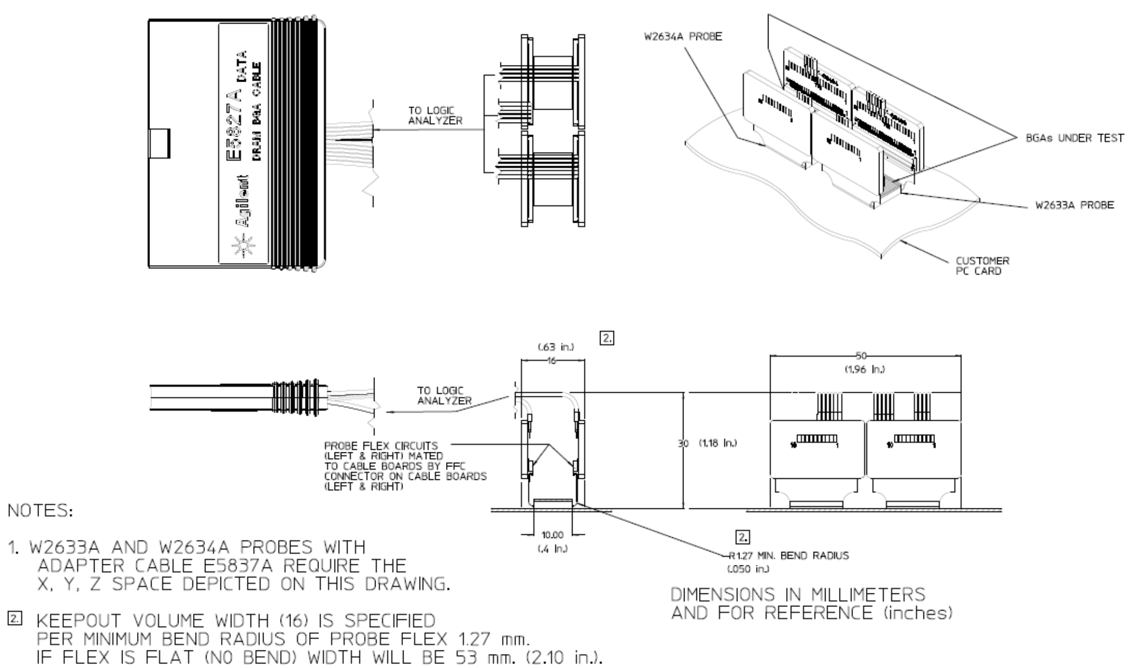

Figure 5 KOV of W2633A, W2634A and E5827A

The following figure shows the dimensions of the Agilent W2631A, W2632A, W2633A and W2634A DRAM BGA probes.

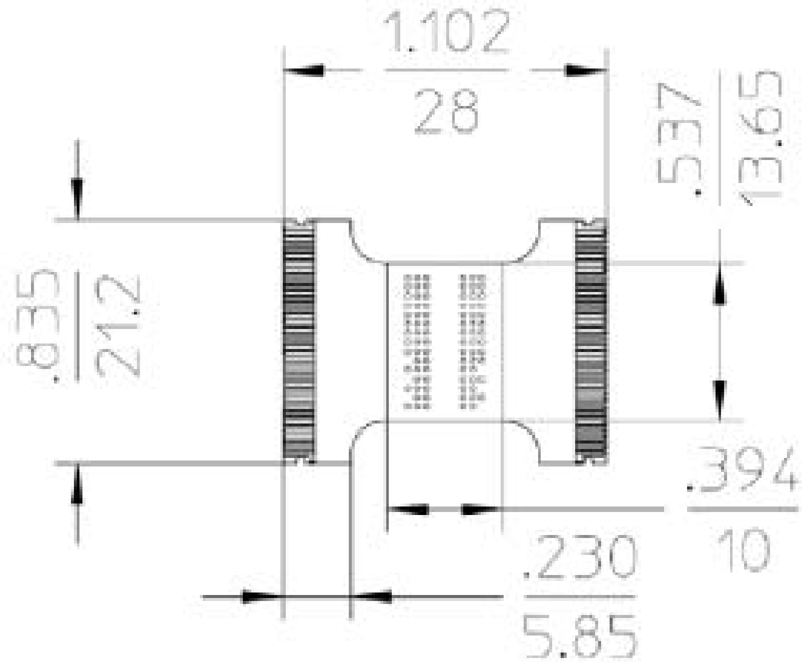

Figure 6 W2631/2/3/4A probe dimensions

2 Installing the Probe

Soldering the probe

The W2631/2/3/4 BGA probes need to be attached to the DRAM PCB footprint on the design to be probed, and the desired DRAM is soldered to the top side of the probe. This attachment may occur in any order (i.e. first solder the probe to the DUT, and then solder the DRAM to the probe, or first solder the DRAM to the probe, and then solder the DRAM+probe assembly to the DUT). The probe is design to tolerate lead-free soldering temperature profiles. However, it is always recommended to apply the minimum temperature required and the minimum number of heating/cooling cycles to reduce risk of any damage to the probe.

The probe is supplied without solder balls. Depending on the exact attachment order, either leaded or lead-free solder may be preferred to attach the probe to the DUT. The design of the probe supports either choice.

The flexible "wings" on the probe may need to be bent upwards before soldering to avoid mechanical contact with components adjacent to the probe on the DUT. This will also ensure reliable connection when connect to the logic analyzer cable adapters.

If the in-house expertise to attach the BGA probe and DRAM cannot be found, there are Contract Manufacturers with this expertise that may be willing to perform the attachment for a fee. More information on BGA soldering and rework techniques that may be useful in attaching the probe may be found at:

http://www.circuitrework.com/guides/9-0.shtml or
http://www.agilent.com/find/ddr2bga

Logic Analyzer connection to the W2630-series probe

The E5384A and E5826/7A adapter cables are used with the W2630-series BGA probe to connect the probe to the logic analyzer. The E5384A and/or E5826/7A plug into the 90-pin logic analyzer pod cable.

Table 2 Logic Analyzer Channel Mapping for the E5384A Probe Cable

Data Pod		Control Pod		Address Pod	
LA Channel	**Signal Name**	**LA Channel**	**Signal Name**	**LA Channel**	**Signal Name**
0	DQ0	0	CS#	0	SPARE1
1	DQ1	1	CAS#	1	SPARE2
2	DQ2	2	RAS#	2	RFU#2
3	DQ3	3	ODT	3	A12
4	DQ4	4	BA2	4	A11
5	DQ5	5	BA0	5	A10
6	DQ6	6	BA1	6	A9
7	DQ7	7	CKE	7	A8
8	DQ8	8	WE#	8	A7
9	DQ9	9	VREF	9	A6
10	DQ10	10	LDM	10	A5
11	DQ11	11	UDM	11	A4
12	DQ12	12	-	12	A3
13	DQ13	13	-	13	A2
14	DQ14	14	-	14	A1
15	DQ15	15	-	15	A0
Clock_P	LDQS	Clock_P	CK	Clock_P	-
Clock_N	LDQS#	Clock_N	CK#	Clock_N	-

Table 3 Logic Analyzer Channel Mapping for the E5826A Probe Cable

Data Pod	
LA Channel	**Signal Name**
0	DQ0
1	DQ1
2	DQ2
3	DQ3
4	DQ4
5	DQ5
6	DQ6
7	DQ7
8	DQ8
9	DQ9
10	DQ10
11	DQ11
12	DQ12
13	DQ13
14	DQ14
15	DQ15
Clock_P	LDQS
Clock_N	LDQS#

Table 4 Logic Analyzer Channel Mapping for the E5827A Probe Cable

Data Pod	
LA Channel	**Signal Name**
0	DQ0 (Probe #1)
1	DQ1 (Probe #1)
2	DQ2 (Probe #1)
3	DQ3 (Probe #1)
4	DQ4 (Probe #1)
5	DQ5 (Probe #1)
6	DQ6 (Probe #1)
7	DQ7 (Probe #1)
8	DQ0 (Probe #2)
9	DQ3 (Probe #2)
10	DQ2 (Probe #2)
11	DQ1 (Probe #2)
12	DQ6 (Probe #2)
13	DQ5 (Probe #2)
14	DQ4 (Probe #2)
15	DQ7 (Probe #2)
Clock_P	LDQS (Probe #1)
Clock_N	LDQS# (Probe #1)

Scope connection to the W2630-series probe

The DDR2 BGA probe is used with the solder-in probe N5381A or E2677A high bandwidth solder in probe to connect to the scope. The solder in probe makes a 2GHz bandwidth connection with the solder points on the BGA probe. The other alternative is to solder the ZIF probe head onto the soldering points on the flex cable and probe with the N5426A ZIF tip.

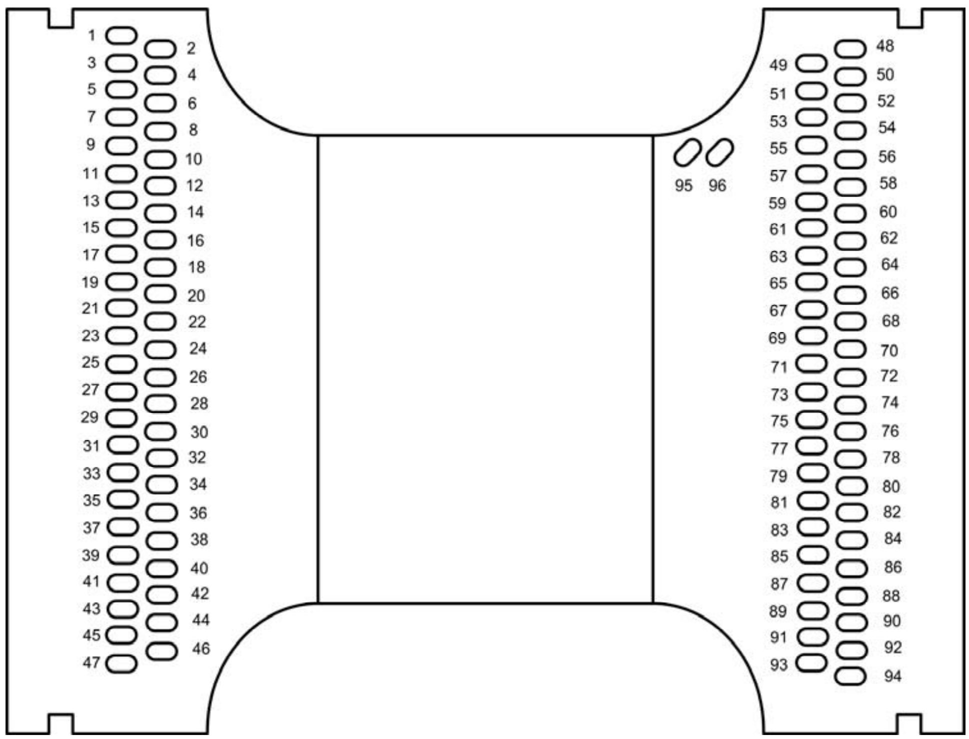

Figure 7 W2631A Scope Pad Numbering as seen through the board from the topside of the probe

Table 5 W2631A Scope Pad Numbering

Pin #		Signal Name	
1		GND	
	2		UDM
3		GND	
	4		DQ14
5		GND	
	6		DQ9
7		GND	

Signal Name		Pin #	
	GND		48
DQ15		49	
	GND		50
DQ8		51	
	GND		52
DQ10		53	
	GND		54

Pin #		Signal Name	
	8		DQ11
9		GND	
	10		DQ12
11		GND	
	12		LDM
13		GND	
	14		DQ6
15		GND	
	16		DQ1
17		GND	
	18		DQ3
19		GND	
	20		DQ4
21		GND	
	22		VREF
23		GND	
	24		WE#
25		GND	
	26		CKE
27		GND	
	28		BA1
29		GND	
	30		BA0
31		GND	
	32		BA2
33		GND	
	34		A1
35		GND	
	36		A10
37		GND	
	38		A5
39		GND	
	40		A3
41		GND	
	42		A7
43		GND	
	44		A9
45		GND	
	46		A12
47		GND	

Signal Name		Pin #	
DQ13		55	
	GND		56
LDQS#		57	
	GND		58
LDQS		59	
	GND		60
DQ7		61	
	GND		62
DQ0		63	
	GND		64
DQ2		65	
	GND		66
DQ5		67	
	GND		68
CK		69	
	GND		70
CK#		71	
	GND		72
ODT		73	
	GND		74
RAS#		75	
	GND		76
CAS#		77	
	GND		78
CS#		79	
	GND		80
A0		81	
	GND		82
A2		83	
	GND		84
A4		85	
	GND		86
A6		87	
	GND		88
A8		89	
	GND		90
RFU#2		91	
	GND		92
A11		93	
	GND		94

UDQS#			95
UDQS			96

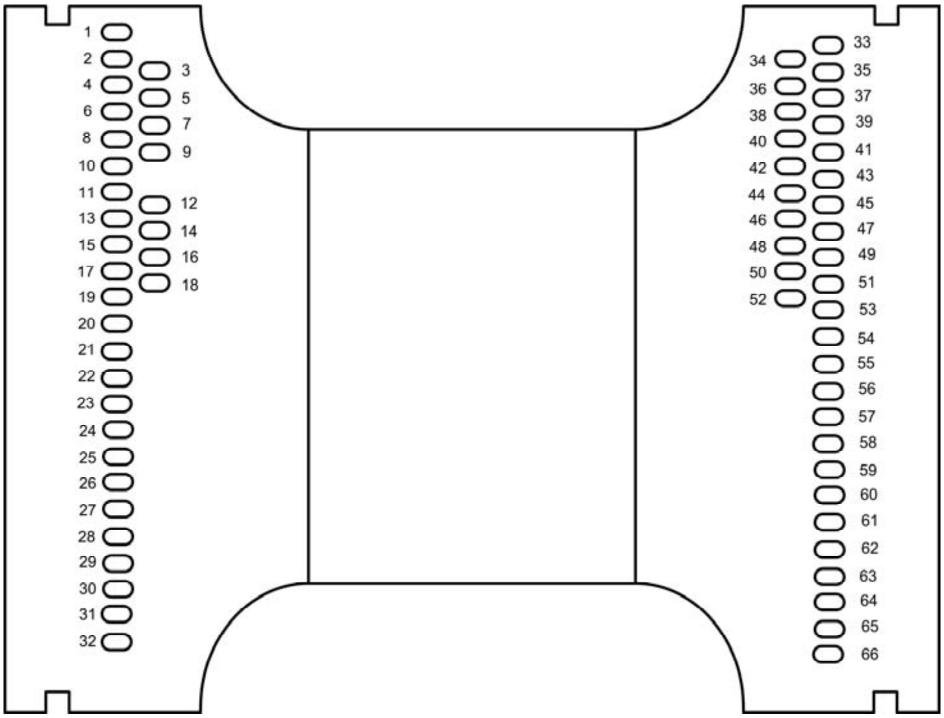

Figure 8 W2632A Scope Pad Numbering as seen through the board from the topside of the probe

Table 6 W2632A Scope Pad Numbering

Pin #		Signal Name	
1		GND	
2		GND	
	3		DQ14
4		GND	
	5		DQ9
6		GND	
	7		DQ11
8		GND	
	9		DQ12
10		GND	
11		GND	

Signal Name		Pin #	
	GND		33
DQ15		34	
	GND		35
DQ8		36	
	GND		37
DQ10		38	
	GND		39
DQ13		40	
	GND		41
LDQS#		42	
	GND		43
LDQS		44	
	GND		45

Pin #		Signal Name	
	12		DQ6
13		GND	
	14		DQ1
15		GND	
	16		DQ3
17		GND	
	18		DQ4
19		GND	
20		GND	
21		GND	
22		GND	
23		GND	
24		GND	
25		GND	
26		GND	
27		GND	
28		GND	
29		GND	
30		GND	
31		GND	
32		GND	

Signal Name		Pin #	
DQ7		46	
	GND		47
DQ0		48	
	GND		49
DQ2		50	
	GND		51
DQ5		52	
	GND		53
	GND		54
	GND		55
	GND		56
	GND		57
	GND		58
	GND		59
	GND		60
	GND		61
	GND		62
	GND		63
	GND		64
	GND		65
	GND		66

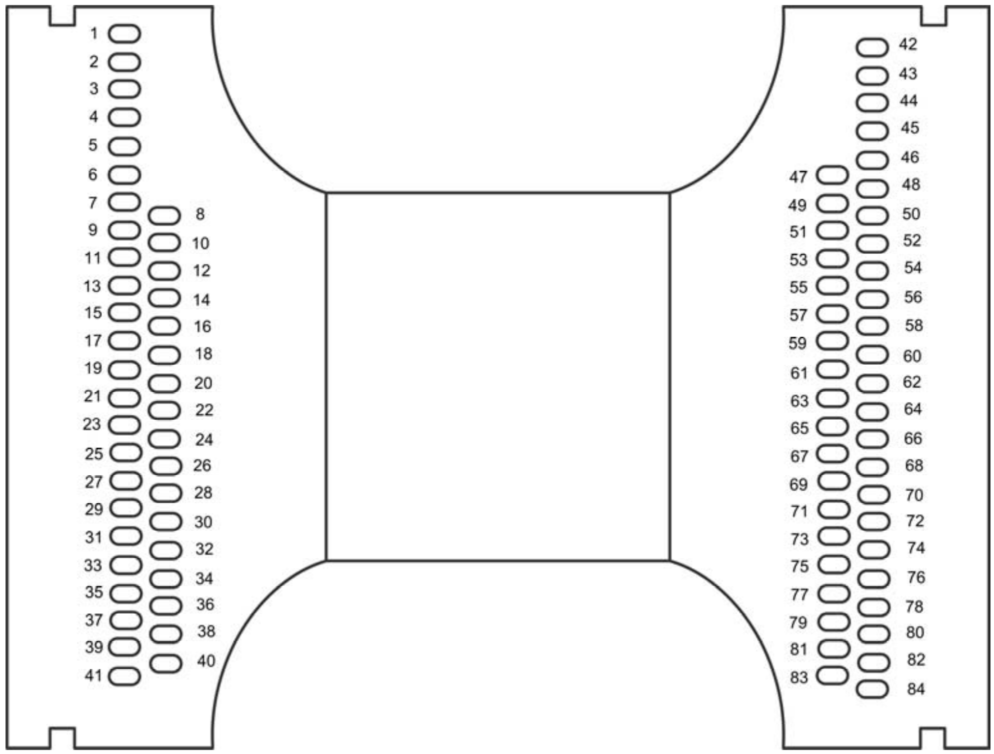

Figure 9 W2633A Scope Pad Numbering as seen through the board from the topside of the probe

Table 7 W2633A Scope Pad Numbering

Pin #		Signal Name	
1		GND	
2		GND	
3		GND	
4		GND	
5		GND	
6		GND	
7		GND	
	8		DQ6

Signal Name		Pin #	
	GND		42
	GND		43
	GND		44
	GND		45
	GND		46
LDQS#		47	
	GND		48
LDQS		49	
	GND		50
DQ7		51	

Pin #		Signal Name	
9		GND	
	10		DQ1
11		GND	
	12		DQ3
13		GND	
	14		DQ4
15		GND	
	16		VREF
17		GND	
	18		WE#
19		GND	
	20		CKE
21		GND	
	22		BA1
23		GND	
	24		BA0
25		GND	
	26		BA2
27		GND	
	28		A1
29		GND	
	30		A10
31		GND	
	32		A5
33		GND	
	34		A3
35		GND	
	36		A7
37		GND	
	38		A9
39		GND	
	40		A12
41		GND	

Signal Name		Pin #	
	GND		52
DQ0		53	
	GND		54
DQ2		55	
	GND		56
DQ5		57	
	GND		58
CK		59	
	GND		60
CK#		61	
	GND		62
ODT		63	
	GND		64
RAS#		65	
	GND		66
CAS#		67	
	GND		68
CS#		69	
	GND		70
A0		71	
	GND		72
A2		73	
	GND		74
A4		75	
	GND		76
A6		77	
	GND		78
A8		79	
	GND		80
RFU#2		81	
	GND		82
A11		83	
	GND		84

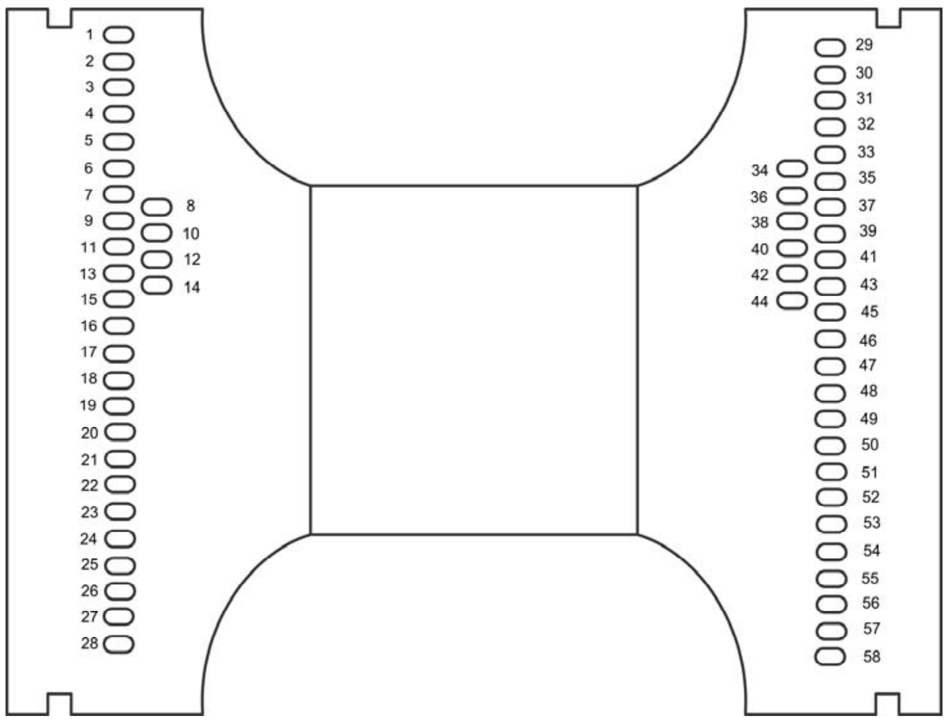

Figure 10 W2634A Scope Pad Numbering as seen through the board from the topside of the probe

Table 8 W2634A Scope Pad Numbering

Pin #		Signal Name	
1		GND	
2		GND	
3		GND	
4		GND	
5		GND	
6		GND	
7		GND	
	8		DQ6

Signal Name		Pin #	
	GND		29
	GND		30
	GND		31
	GND		32
	GND		33
LDQS#		34	
	GND		35
LDQS		36	
	GND		37
DQ7		38	

Pin #		Signal Name	
9		GND	
	10		DQ1
11		GND	
	12		DQ3
13		GND	
	14		DQ4
15		GND	
16		GND	
17		GND	
18		GND	
19		GND	
20		GND	
21		GND	
22		GND	
23		GND	
24		GND	
25		GND	
26		GND	
27		GND	
28		GND	

Signal Name		Pin #	
	GND		39
DQ0		40	
	GND		41
DQ2		42	
	GND		43
DQ5		44	
	GND		45
	GND		46
	GND		47
	GND		48
	GND		49
	GND		50
	GND		51
	GND		52
	GND		53
	GND		54
	GND		55
	GND		56
	GND		57
	GND		58

3 Setting Up the Logic Analysis System

The mapping of specific signals to logic analyzer channels depends on:

- Which DRAMs on a DIMM are probed
- Which probe you are using
- How the single ended logic analyzer cable adapters are arranged when connecting to the DDR2 DRAM BGA probe

Because of these dependencies, there is no single logic analyzer configuration file setup, and no configuration file is supplied with the probes. The logic analyzer Buses/Signals setup dialog will allow you to assign descriptive labels to each analyzer channel that associate each channel with the particular DRAM and DRAM signal being probed.

To save a configuration file

After you set up the logic analyzer, it is strongly recommended that you save the configuration.

To save your work, select **File>Save As...** and save the configuration as an ALA format file.

ALA format configuration files are more complete and efficient than XML format configuration files. See the logic analyzer online help for more information on these formats.

4 Characteristics, Regulatory, and Safety Information

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics.

Table 9 Electrical Characteristics (W2631A, W2632A, W2633A, W2634A)

Operating Transfer Rate	800 Mb/s
Bandwidth (f_{-3dB})	1 GHz
Rise time	350 ps
Input Impedance	
- with Logic Cables Attached	20k Ω
- with Infiinimax Scope Probe Attached	25k Ω
Input Impedance	

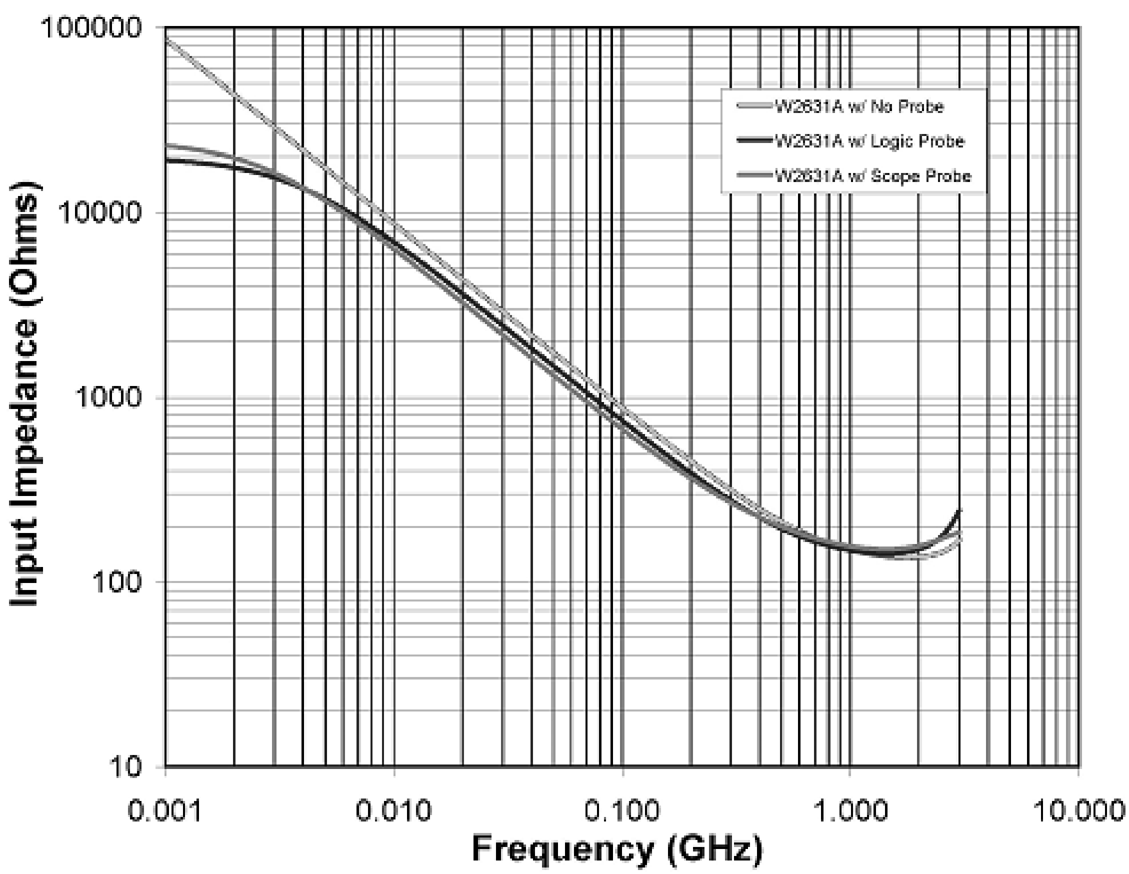

Figure 11 Input Impedance of W2631/32/33/34A Probes (with and without instrument probe connections)

NOTES: Logic probe connection made using either the E5384A, E5826A, or E5827A Probe Cables.
Scope probe connection made using the Infiniimax N5425A ZIF Probe with the N5426A tip attached.

Load Model

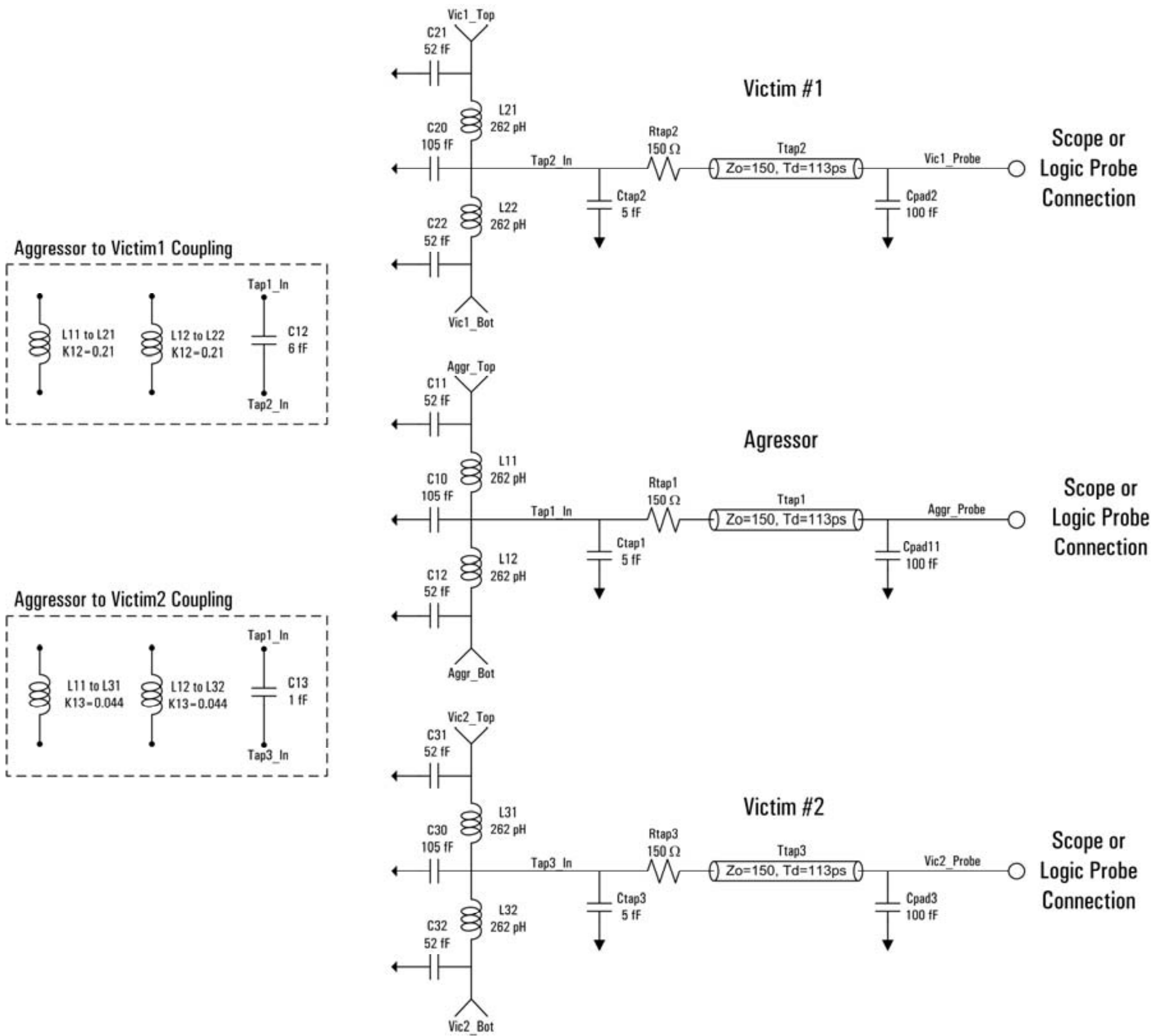

Figure 12 Load Model of W2631/32/33/34A Probes (not showing instrument load)

SPICE Deck of Load Model

Without Probe

```
****************************************************************************************************
*** Equivalent Load Model : W2631A, W2632A, W2633 and W2634A DDR2 Interposer Probes with No Probe
*** June 2007
*** Rev001
***
***       This SPICE subcircuit models the input impedance of the W2631A, W2632A, W2633 and W2634A DDR2
***       interposer probes.  This models the effect of the probe loading on the system.
***       This is a 3-line model which includes mutual inductive and capacitive coupling from
***       one aggressing line to two adjacent victim pins (K12 & K13).
***       This model is accurate up to 3GHz for input impedance simulations.
***
***     Port Description:
***
***          Aggr_Top         = Top pad of the interposer for the aggressor line
***          Aggr_Bot         = Bottom pad of the interposer for the aggressor line
***          Aggr_Probe = Probe pad along perimeter of the interposer for the aggressor line
***          Vic1_Top         = Top pad of the interposer for the Victim #1 line (K12, C12)
***          Vic1_Bot         = Bottom pad of the interposer for the Victim #1 line (K12, C12)
***          Vic1_Probe = Probe pad along perimeter of the interposer for the Victim #1 line (13)
***          Vic2_Top         = Top pad of the interposer for the Victim #2 line (K12, C12)
***          Vic2_Bot         = Bottom pad of the interposer for the Victim #2 line (K12, C12)
***          Vic2_Probe = Probe pad along perimeter of the interposer for the Victim #2 line (13)
***
***            NOTE:  The probe ground is assumed to be ideal and is labeled node 0
***            NOTE:  K23, C23 is negligible
***
***       This model is used to simulate the load of the interposer with no logic analyzer
***     or oscilloscope attached.
****************************************************************************************************

.subckt W2631_RevA1_Model_NoProbe_SUBCKT
+ Aggr_Top Aggr_Bot Aggr_Probe
+ Vic1_Top Vic1_Bot Vic1_Probe
+ Vic2_Top Vic2_Bot Vic2_Probe

.param Zint=50
.param Tint='(169p)*0.062'
.param Lint='Zint*Tint'
.param Cint='Tint/Zint'
.param K12=0.21
.param K13=0.044
.param C12=6f
.param C13=1f
.param Rtap=150
.param Ctap=5f
.param Ztap=75
.param Ttap='(169p)*0.67'
.param Cpad1=100f

CC10 0 Tap1_In C='Cint/2'
CC11 0 Aggr_Top C='Cint/4'
CC12 0 Aggr_Bot C='Cint/4'
CC20 0 Tap2_In C='Cint/2'
CC21 0 Vic1_Top C='Cint/4'
CC22 0 Vic1_Bot C='Cint/4'
CC30 0 Tap3_In C='Cint/2'
CC31 0 Vic2_Top C='Cint/4'
CC32 0 Vic2_Bot C='Cint/4'
CCcouple12 Tap2_In Tap1_In C=C12
CCcouple13 Tap3_In Tap1_In C=C13
CCpad1 0 Aggr_Probe C=Cpad1
CCpad2 0 Vic1_Probe C=Cpad1
CCpad3 0 Vic2_Probe C=Cpad1
CCtap1 0 Tap1_In C=Ctap
CCtap2 0 Tap2_In C=Ctap
CCtap3 0 Tap3_In C=Ctap
LL11 Aggr_Top Tap1_In 'Lint/2'
LL12 Tap1_In Aggr_Bot 'Lint/2'
LL21 Vic1_Top Tap2_In 'Lint/2'
LL22 Tap2_In Vic1_Bot 'Lint/2'
LL31 Vic2_Top Tap3_In 'Lint/2'
LL32 Tap3_In Vic2_Bot 'Lint/2'
RRtap1 Tap1_In _net4577 Rtap
RRtap2 Tap2_In _net4578 Rtap
RRtap3 Tap3_In _net4540 Rtap
TTtap1 _net4577 Aggr_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap2 _net4578 Vic1_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap3 _net4540 Vic2_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'

.ends W2631_RevA1_Model_NoProbe_SUBCKT
```

With Logic Probe

```
*****************************************************************************************************
*** Equivalent Load Model : W2631A, W2632A, W2633 and W2634A DDR2 Interposer Probes with Logic Probe Attached
*** June 2007
*** Rev001
***
***       This SPICE subcircuit models the input impedance of the W2631A, W2632A, W2633 and W2634A DDR2
***       interposer probes.  This models the effect of the probe loading on the system.
***       This is a 3-line model which includes mutual inductive and capacitive coupling from
***       one aggressing line to two adjacent victim pins (K12 & K13).
***       This model is accurate up to 3GHz for input impedance simulations.
***
***     Port Description:
***          Aggr_Top         = Top pad of the interposer for the aggressor line
***          Aggr_Bot         = Bottom pad of the interposer for the aggressor line
***          Aggr_Probe = Probe pad along perimeter of the interposer for the aggressor line
***          Vic1_Top         = Top pad of the interposer for the Victim #1 line (K12, C12)
***          Vic1_Bot         = Bottom pad of the interposer for the Victim #1 line (K12, C12)
***          Vic1_Probe = Probe pad along perimeter of the interposer for the Victim #1 line (K13, C13)
***          Vic2_Top         = Top pad of the interposer for the Victim #2 line (K12, C12)
***          Vic2_Bot         = Bottom pad of the interposer for the Victim #2 line (K12, C12)
***          Vic2_Probe = Probe pad along perimeter of the interposer for the Victim #2 line (K13, C13)
***
***            NOTE:  The probe ground is assumed to be ideal and is labeled node 0
***            NOTE:  K23, C23 is negligible
***
***       This model is used to simulate the load of the interposer with a logic analyzer attached
***     using either the E5384A, E5826A, or E5827A adapter cables.
*****************************************************************************************************

.subckt W2631_RevA1_Model_LogicProbe_SUBCKT
+ Aggr_Top Aggr_Bot Aggr_Probe
+ Vic1_Top Vic1_Bot Vic1_Probe
+ Vic2_Top Vic2_Bot Vic2_Probe

.param Rtip=20k
.param Ctip=350f
.param Rterm=75
.param Vterm=0.7
.param Zint=50
.param Tint='(169p)*0.062'
.param Lint='Zint*Tint'
.param Cint='Tint/Zint'
.param K12=0.21
.param K13=0.044
.param C12=6f
.param C13=1f
.param Rtap=150
.param Ctap=5f
.param Ztap=75
.param Ttap='(169p)*0.67'
.param Cpad1=100f

CC10 0 Tap1_In C='Cint/2'
CC11 0 Aggr_Top C='Cint/4'
CC12 0 Aggr_Bot C='Cint/4'
CC20 0 Tap2_In C='Cint/2'
CC21 0 Vic1_Top C='Cint/4'
CC22 0 Vic1_Bot C='Cint/4'
CC30 0 Tap3_In C='Cint/2'
CC31 0 Vic2_Top C='Cint/4'
CC32 0 Vic2_Bot C='Cint/4'
CCcouple12 Tap2_In Tap1_In C=C12
CCcouple13 Tap3_In Tap1_In C=C13
CCpad1 0 Aggr_Probe C=Cpad1
CCpad2 0 Vic1_Probe C=Cpad1
CCpad3 0 Vic2_Probe C=Cpad1
CCtap1 0 Tap1_In C=Ctap
CCtap2 0 Tap2_In C=Ctap
CCtap3 0 Tap3_In C=Ctap
CCtip1 _net4688 Aggr_Probe C=Ctip
CCtip2 _net4697 Vic1_Probe C=Ctip
CCtip3 _net4707 Vic2_Probe C=Ctip
LL11 Aggr_Top Tap1_In 'Lint/2'
LL12 Tap1_In Aggr_Bot 'Lint/2'
LL21 Vic1_Top Tap2_In 'Lint/2'
LL22 Tap2_In Vic1_Bot 'Lint/2'
LL31 Vic2_Top Tap3_In 'Lint/2'
LL32 Tap3_In Vic2_Bot 'Lint/2'
RRtap1 Tap1_In _net4577 Rtap
RRtap2 Tap2_In _net4578 Rtap
RRtap3 Tap3_In _net4540 Rtap
RRterm1 _net4688 _net4689 Rterm
RRterm2 _net4697 _net4699 Rterm
RRterm3 _net4707 _net4708 Rterm
RRtip1 Aggr_Probe _net4688 Rtip
RRtip2 Vic1_Probe _net4697 Rtip
RRtip3 Vic2_Probe _net4707 Rtip
TTtap1 _net4577 Aggr_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap2 _net4578 Vic1_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap3 _net4540 Vic2_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
VVterm1 _net4689 0 Vterm
VVterm2 _net4699 0 Vterm
VVterm3 _net4708 0 Vterm

.ends W2631_RevA1_Model_LogicProbe_SUBCKT
```

With Scope Probe

```
****************************************************************************************************
*** Equivalent Load Model : W2631A, W2632A, W2633 and W2634A DDR2 Interposer Probes with Oscilloscope Probe
*** June 2007
*** Rev001
***
***       This SPICE subcircuit models the input impedance of the W2631A, W2632A, W2633 and W2634A DDR2
***       interposer probes.  This models the effect of the probe loading on the system.
***       This is a 3-line model which includes mutual inductive and capacitive coupling from
***       one aggressing line to two adjacent victim pins (K12 & K13).
***       This model is accurate up to 3GHz for input impedance simulations.
***
***     Port Description:
***
***          Aggr_Top         = Top pad of the interposer for the aggressor line
***          Aggr_Bot         = Bottom pad of the interposer for the aggressor line
***          Aggr_Probe = Probe pad along perimeter of the interposer for the aggressor line
***          Vic1_Top         = Top pad of the interposer for the Victim #1 line (K12, C12)
***          Vic1_Bot         = Bottom pad of the interposer for the Victim #1 line (K12, C12)
***          Vic1_Probe = Probe pad along perimeter of the interposer for the Victim #1 line (K13, C13)
***          Vic2_Top         = Top pad of the interposer for the Victim #2 line (K12, C12)
***          Vic2_Bot         = Bottom pad of the interposer for the Victim #2 line (K12, C12)
***          Vic2_Probe = Probe pad along perimeter of the interposer for the Victim #2 line (K13, C13)
***
***            NOTE:  The probe ground is assumed to be ideal and is labeled node 0
***            NOTE:  K23, C23 is negligible
***
***       This model is used to simulate the load of the interposer with the Agilent N5425A ZIF Probe head
***     with the N5426A ZIF Tip attached and soldered to the observation pads on the interposer.
***
***
****************************************************************************************************

.subckt W2631_RevA1_Model_ScopeProbe_SUBCKT
+ Aggr_Top Aggr_Bot Aggr_Probe
+ Vic1_Top Vic1_Bot Vic1_Probe
+ Vic2_Top Vic2_Bot Vic2_Probe

.param Zint=50
.param Tint='(169p)*0.062'
.param Lint='Zint*Tint'
.param Cint='Tint/Zint'
.param K12=0.21
.param K13=0.044
.param C12=6f
.param C13=1f

.param Rtap=150
.param Ctap=5f
.param Ztap=75
.param Ttap='(169p)*0.67'
.param Cpad1=100f

CC1 _net4933 _net4991 C=14.75fF
CC10 0 Tap1_In C='Cint/2'
CC11 0 Aggr_Top C='Cint/4'
CC12 0 Aggr_Bot C='Cint/4'
CC2 _net4941 _net4991 C=6.3fF
CC20 0 Tap2_In C='Cint/2'
CC21 0 Vic1_Top C='Cint/4'
CC22 0 Vic1_Bot C='Cint/4'
CC30 0 Tap3_In C='Cint/2'
CC31 0 Vic2_Top C='Cint/4'
CC32 0 Vic2_Bot C='Cint/4'
CC33 _net5160 _net5186 C=6.3fF
CC34 _net5152 _net5186 C=14.75fF
CC35 _net5309 _net5335 C=6.3fF
CC36 _net5301 _net5335 C=14.75fF
CCcouple12 Tap2_In Tap1_In C=C12
CCcouple13 Tap3_In Tap1_In C=C13
CCn1 _net4948 _net5008 C=556.5fF
CCn2 _net4963 _net5008 C=40.93fF
CCn3 _net5182 _net5190 C=40.93fF
CCn4 _net5167 _net5190 C=556.5fF
CCn5 _net5331 _net5339 C=40.93fF
CCn6 _net5316 _net5339 C=556.5fF
CCp1 _net4951 _net5031 C=556.5fF
CCp2 _net4960 _net5031 C=40.93fF
CCp3 _net5179 _net5191 C=40.93fF
CCp4 _net5170 _net5191 C=556.5fF
CCp5 _net5328 _net5340 C=40.93fF
CCp6 _net5319 _net5340 C=556.5fF
CCpad1 0 Aggr_Probe C=Cpad1
CCpad2 0 Vic1_Probe C=Cpad1
CCpad3 0 Vic2_Probe C=Cpad1
CCtap1 0 Tap1_In C=Ctap
CCtap2 0 Tap2_In C=Ctap
CCtap3 0 Tap3_In C=Ctap
LL1 _net4933 _net4936 1.356nH
LL11 Aggr_Top Tap1_In 'Lint/2'
LL12 Tap1_In Aggr_Bot 'Lint/2'
LL2 _net4941 _net4942 345.2pH
LL21 Vic1_Top Tap2_In 'Lint/2'
LL22 Tap2_In Vic1_Bot 'Lint/2'
LL31 Vic2_Top Tap3_In 'Lint/2'
LL32 Tap3_In Vic2_Bot 'Lint/2'
LL33 _net5160 _net5161 345.2pH
LL34 _net5152 _net5155 1.356nH
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LL35 _net5309 _net5310 345.2pH
LL36 _net5301 _net5304 1.356nH
LLn1 _net4948 _net4946 3.815nH
LLn2 _net4963 _net4966 5.731nH
LLn3 _net5182 _net5185 5.731nH
LLn4 _net5167 _net5165 3.815nH
LLn5 _net5331 _net5334 5.731nH
LLn6 _net5316 _net5314 3.815nH
LLom _net5031 0 1uH
LLom2 _net5038 0 2nH
LLom3 _net5193 0 2nH
LLom4 _net5191 0 1uH
LLom5 _net5342 0 2nH
LLom6 _net5340 0 1uH
LLp1 _net4951 _net4954 3.815nH
LLp2 _net4960 _net4958 5.731nH
LLp3 _net5179 _net5177 5.731nH
LLp4 _net5170 _net5173 3.815nH
LLp5 _net5328 _net5326 5.731nH
LLp6 _net5319 _net5322 3.815nH
RR1 _net4936 _net5008 948.2
RR2 _net4942 _net5008 36.88
RR3 _net5161 _net5190 36.88
RR4 _net5155 _net5190 948.2
RR5 _net5310 _net5339 36.88
RR6 _net5304 _net5339 948.2
RRn1 _net4946 _net5031 38.32
RRn2 _net4966 _net5031 30.4
RRn3 _net5008 _net5031 25kOhm
RRn4 _net5190 _net5191 25kOhm
RRn5 _net5185 _net5191 30.4
RRn6 _net5165 _net5191 38.32
RRn7 _net5339 _net5340 25kOhm
RRn8 _net5334 _net5340 30.4
RRn9 _net5314 _net5340 38.32
RRom _net5038 _net5031 250
RRom1 _net5193 _net5191 250
RRom2 _net5342 _net5340 250
RRp1 _net4954 _net4991 38.32
RRp2 _net4958 _net4991 30.4
RRp3 _net5031 _net4991 25kOhm
RRp4 _net5191 _net5186 25kOhm
RRp5 _net5177 _net5186 30.4
RRp6 _net5173 _net5186 38.32
RRp7 _net5340 _net5335 25kOhm
RRp8 _net5326 _net5335 30.4
RRp9 _net5322 _net5335 38.32
RRtap1 Tap1_In _net4577 Rtap
RRtap2 Tap2_In _net5076 Rtap
RRtap3 Tap3_In _net5224 Rtap
RRtipn 0 _net5008 64.35
RRtipn1 0 _net5190 64.35
RRtipn2 0 _net5339 64.35
RRtipp Aggr_Probe _net4991 64.35
RRtipp1 Vic1_Probe _net5186 64.35
RRtipp2 Vic2_Probe _net5335 64.35
TTtap1 _net4577 Aggr_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap2 _net5076 Vic1_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'
TTtap3 _net5224 Vic2_Probe 0 0 Z=Ztap E=360 F='1/(Ttap)'

.ends W2631_RevA1_Model_ScopeProbe_SUBCKT
```

Table 10 Environmental Characteristics (Operating)

Temperature	20° to + 30° C (+68° to +86° F)
Altitude	4,600 m (15,000 ft)
Humidity	Up to 50% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only.

Table 11 Inputs and Outputs

To interposer	Memory bus signals from target system
From interposer	High-density connectors for Agilent logic analyzer cards in an Agilent 16900-series logic analysis system and for an oscilloscope

Safety Notices for the E5384A, E5826A, and E5827A Cable Adapters

This apparatus has been designed and tested in accordance with IEC Publication 61010-1, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

Use only the recommended power supply.

If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do not install substitute parts or perform any unauthorized modification to the instrument.

Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

Do not attempt to clean this product.

Safety Symbols

"Caution" or "Warning" risk of danger marked on product. See"Safety Notices" on page 2 and refer to this manual for a description of the specific danger.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Regulatory Notices

WEEE Compliance

This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste.

Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as a "Monitoring and Control Instrumentation" product.

Do not dispose in domestic household waste.

To return unwanted products, contact your local Agilent office, or see www.agilent.com for more information.

China RoHS

W2631A, W2632A, W2633A and W2634A

E5384A, E5826A and E5827A